CLAIMS

1. A method of processing a semiconductor structure comprising:

providing a substrate;

depositing a lattice-mismatched first layer on said substrate;

annealing said first layer at a temperature greater than 100°C above the deposition temperature; and

depositing a second layer on said first layer with a greater lattice mismatch to said substrate than said first layer.

2. The method of claim 1, wherein said substrate has at least a surface layer comprising Si and said first and second layers comprise $Si_{1-x}Ge_x$.

3. The method of claim 1, wherein said substrate has at least a surface layer comprising GaAs and said first and second layers comprise $In_yGa_{1-y}As$.

4. The method of claim 1, wherein said substrate has at least a surface layer comprising GaP and said first and second layers comprise $In_zGa_{1-z}P$.

5. The method of claim 2, wherein said first and second layers differ by a Ge concentration less than 10% Ge.

6. The method of claim 2, wherein said first and second layers differ in Ge concentration

by approximately 1.5% Ge.

7. The method of claim 2, wherein said first and second layers of $Si_{1-x}Ge_x$ are deposited at a growth temperature less than 850°C.

8. The method of claim 2, wherein said annealing occurs at a temperature greater than 900°C.

9. The method of claim 2, wherein anneal time is greater than 0.1 seconds.

10. The method of claim 2, wherein said first and second layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the anneal temperature is approximately 1050°C.

11. The method of claim 2, wherein said first and second layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the anneal temperature is approximately 1050°C, and the anneal time is greater than 0.1 seconds.

12. The method of claim 1, wherein said lattice-mismatched semiconductor layer is deposited by chemical vapor deposition.

13. A method of processing a semiconductor graded composition layer structure on a

semiconductor substrate comprising:

providing a semiconductor substrate;

depositing a first layer having a series of lattice-mismatched semiconductor layers on said substrate;

annealing said layer at a temperature greater than 100°C above the deposition temperature;

depositing a second layer on said first layer with a greater lattice mismatch to said substrate than said first layer; and

annealing said second layer at a temperature greater than 100°C above the deposition temperature of said second layer.

14. The method of claim 13, wherein said substrate has at least a surface layer comprising Si and said first and second layers comprise $Si_{1-x}Ge_x$.

15. The method of claim 13, wherein said substrate has at least a surface layer comprising GaAs and said first and second layers comprise $In_yGa_{1-y}As$.

16. The method of claim 13, wherein said substrate has at least a surface layer comprising GaP and said first and second layers comprise $In_zGa_{1-z}P$.

17. The method of claim 14, wherein sequential layers in the graded composition layers differ by a Ge concentration less than 10% Ge.

18. The method of claim 14, wherein sequential layers in the graded composition layers differ in Ge concentration by approximately 1.5% Ge.

19. The method of claim 14, wherein said first layer and second layers are deposited at a growth temperature of less than 850°C.

20. The method of claim 14, wherein said annealing occurs at a temperature greater than 900°C.

21. The method of claim 14, wherein anneal time is greater than 0.1 seconds.

22. The method of claim 14, wherein sequential layers in the graded composition layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the anneal temperature is approximately 1050°C.

23. The method of claim 14, wherein sequential layers in the graded composition layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the anneal temperature is approximately 1050°C, and the anneal time is greater than 0.1 seconds.

24. The method of claim 13, wherein said lattice-mismatched semiconductor layer is deposited by chemical vapor deposition.